

# BUK9880-55A

TrenchMOS™ logic level FET

Rev. 01 — 07 February 2001

Product specification

## 1. Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™<sup>1</sup> technology, featuring very low on-state resistance.

Product availability:

BUK9880-55A in SOT223 (SC-73).

## 2. Features

- TrenchMOS™ technology
- Q101 compliant
- 150 °C rated
- Logic level compatible.

## 3. Applications

- Automotive and general purpose power switching:
  - ◆ 12 V and 24 V loads
  - ◆ Motors, lamps and solenoids.

## 4. Pinning information

Table 1: Pinning - SOT223 (SC-73), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	<p>Top view</p> <p>MSB002 - 1</p> <p><b>SOT223 (SC-73)</b></p>	<p>MBB076</p>
2	drain (d)		
3	source (s)		
4	drain (d)		

1. TrenchMOS is a trademark of Royal Philips Electronics.



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## 5. Quick reference data

**Table 2: Quick reference data**

Symbol	Parameter	Conditions	Typ	Max	Unit
$V_{DS}$	drain-source voltage (DC)		–	55	V
$I_D$	drain current (DC)	$T_{sp} = 25\text{ °C}; V_{GS} = 5\text{ V}$	–	7	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C}$	–	8	W
$T_j$	junction temperature		–	150	°C
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 8\text{ A}; T_j = 25\text{ °C}$	68	80	mΩ
		$V_{GS} = 4.5\text{ V}; I_D = 8\text{ A}; T_j = 25\text{ °C}$	–	89	mΩ
		$V_{GS} = 10\text{ V}; I_D = 8\text{ A}; T_j = 25\text{ °C}$	–	73	mΩ

## 6. Limiting values

**Table 3: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

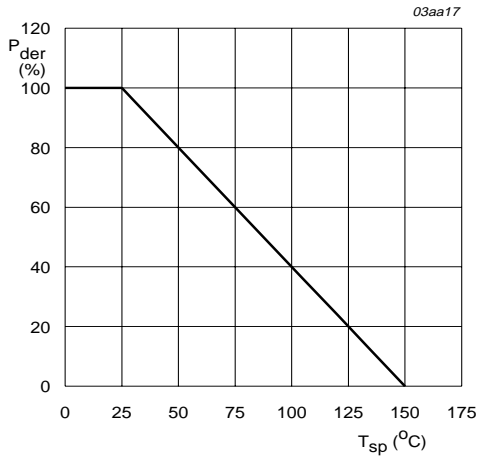
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage (DC)		–	55	V
$V_{DGR}$	drain-gate voltage (DC)	$R_{GS} = 20\text{ k}\Omega$	–	55	V
$V_{GS}$	gate-source voltage (DC)		–	±10	V
$V_{GSM}$	non-repetitive gate-source voltage	$t_p \leq 50\text{ }\mu\text{s}$	–	±15	V
$I_D$	drain current (DC)	$T_{sp} = 25\text{ °C}; V_{GS} = 5\text{ V};$ <b>Figure 2 and 3</b>	–	7	A
		$T_{sp} = 100\text{ °C}; V_{GS} = 5\text{ V};$ <b>Figure 2</b>	–	4	A
$I_{DM}$	peak drain current	$T_{sp} = 25\text{ °C};$ pulsed $t_p \leq 10\text{ }\mu\text{s};$ <b>Figure 3</b>	–	30	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C};$ <b>Figure 1</b>	–	8	W
$T_{stg}$	storage temperature		–55	+150	°C
$T_j$	operating junction temperature		–55	+150	°C

### Source-drain diode

$I_{DR}$	reverse drain current (DC)	$T_{sp} = 25\text{ °C}$	–	7	A
$I_{DRM}$	pulsed reverse drain current	$T_{sp} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s}$	–	30	A

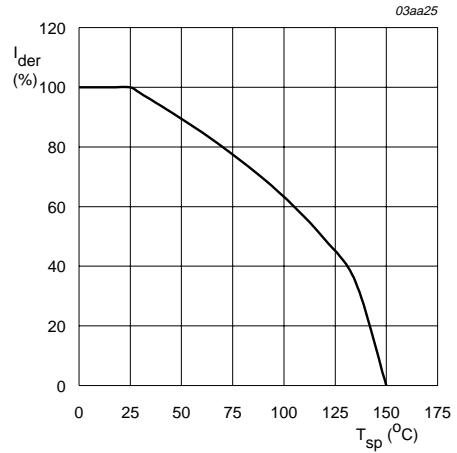
### Avalanche ruggedness

$W_{DSS}$	non-repetitive avalanche energy	unclamped inductive load; $I_D = 6\text{ A};$ $V_{DS} \leq 55\text{ V}; V_{GS} = 5\text{ V}; R_{GS} = 50\text{ }\Omega;$ starting $T_{sp} = 25\text{ °C}$	–	36	mJ
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$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

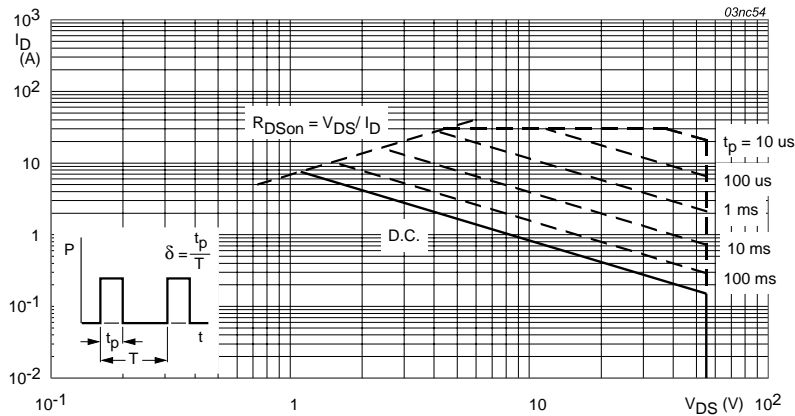
**Fig 1. Normalized total power dissipation as a function of solder point temperature.**



$$V_{GS} \geq 4.5 \text{ V}$$

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

**Fig 2. Normalized continuous drain current as a function of solder point temperature.**



T<sub>amb</sub> = 25 °C; I<sub>DM</sub> is single pulse.

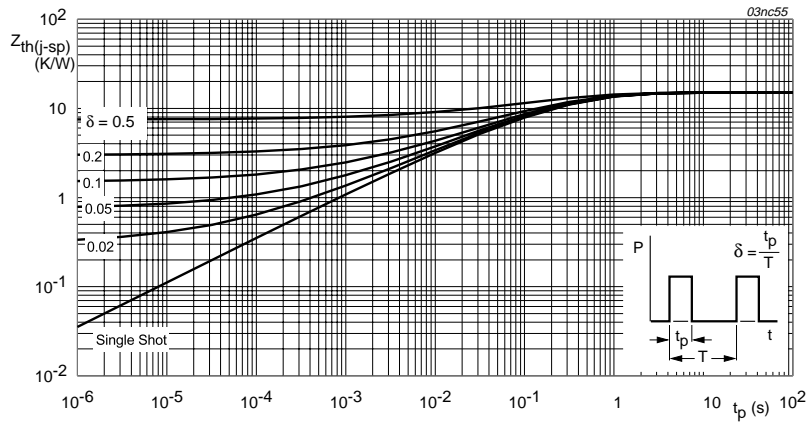
**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.**

## 7. Thermal characteristics

**Table 4: Thermal characteristics**

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	Figure 4	70	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		15	K/W

### 7.1 Transient thermal impedance



**Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration.**

## 8. Characteristics

**Table 5: Characteristics**

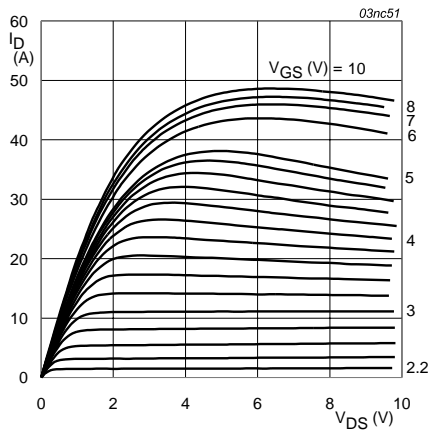
$T_j = 25\text{ °C}$  unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25\text{ mA}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	55	–	–	V
		$T_j = -55\text{ °C}$	50	–	–	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}; V_{DS} = V_{GS};$ <b>Figure 9</b>				
		$T_j = 25\text{ °C}$	1	1.5	2	V
		$T_j = 150\text{ °C}$	0.6	–	–	V
		$T_j = -55\text{ °C}$	–	–	2.3	V
$I_{DSS}$	drain-source leakage current	$V_{DS} = 55\text{ V}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	–	0.05	10	$\mu\text{A}$
		$T_j = 150\text{ °C}$	–	–	500	$\mu\text{A}$
$I_{GSS}$	gate-source leakage current	$V_{GS} = \pm 10\text{ V}; V_{DS} = 0\text{ V}$	–	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 8\text{ A};$ <b>Figure 7 and 8</b>				
		$T_j = 25\text{ °C}$	–	68	80	m $\Omega$
		$T_j = 150\text{ °C}$	–	–	147	m $\Omega$
		$V_{GS} = 4.5\text{ V}; I_D = 8\text{ A};$			89	m $\Omega$
		$V_{GS} = 10\text{ V}; I_D = 8\text{ A};$		62	73	m $\Omega$
<b>Dynamic characteristics</b>						
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V};$ $f = 1\text{ MHz};$ <b>Figure 12</b>	–	438	584	pF
$C_{oss}$	output capacitance		–	87	104	pF
$C_{rss}$	reverse transfer capacitance		–	62	85	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 30\text{ V}; R_L = 1.2\text{ }\Omega;$	–	8	–	ns
$t_r$	rise time	$V_{GS} = 5\text{ V}; R_G = 10\text{ }\Omega$	–	118	–	ns
$t_{d(off)}$	turn-off delay time		–	20	–	ns
$t_f$	fall time		–	32	–	ns

**Table 5: Characteristics...continued**

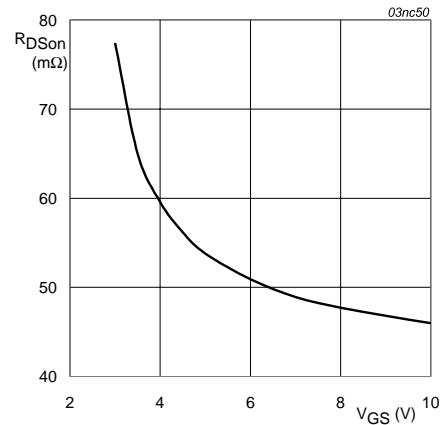
$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$V_{SD}$	source-drain (diode forward) voltage	$I_S = 15\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; <b>Figure 15</b>	–	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20\text{ A}$ ; $dI_S/dt = -100\text{ A}/\mu\text{s}$	–	33	–	ns
$Q_r$	recovered charge	$V_{GS} = -10\text{ V}$ ; $V_{DS} = 30\text{ V}$	–	60	–	nC



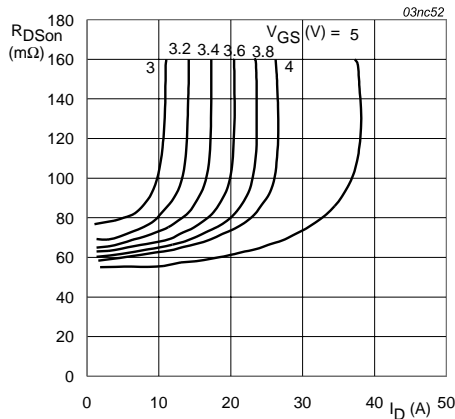
$T_j = 25\text{ }^\circ\text{C}$

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.**



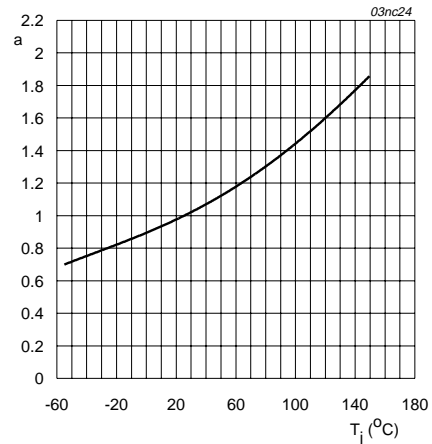
$T_j = 25\text{ }^\circ\text{C}$ ;  $I_D = 10\text{ A}$

**Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.**



$T_j = 25\text{ }^\circ\text{C}$

**Fig 7. Drain-source on-state resistance as a function of drain current; typical values.**



$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.**



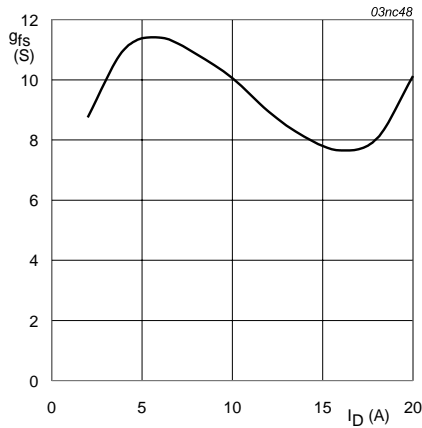
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature.**



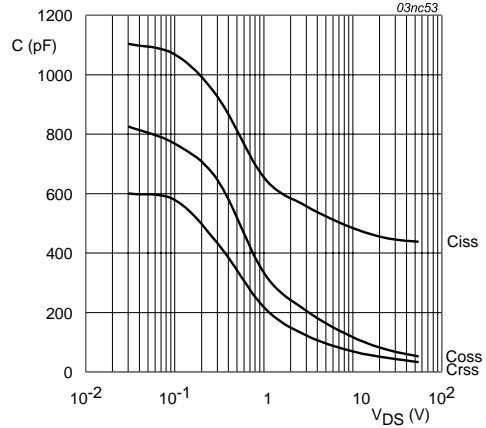
$T_j = 25 \text{ °C}; V_{DS} = V_{GS}$

**Fig 10. Sub-threshold drain current as a function of gate-source voltage.**



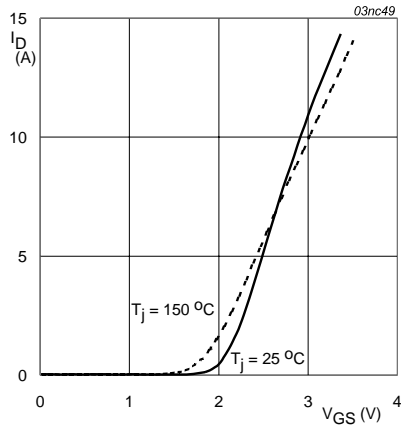
$T_j = 25 \text{ °C}; V_{DS} = 25 \text{ V}$

**Fig 11. Forward transconductance as a function of drain current; typical values.**



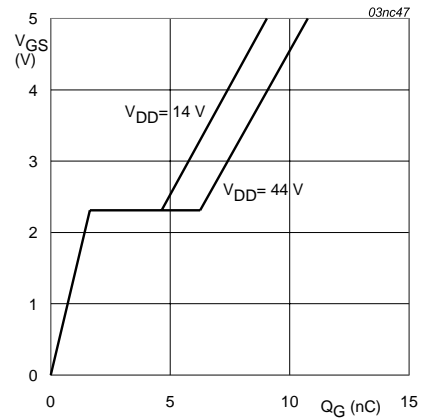
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

**Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.**



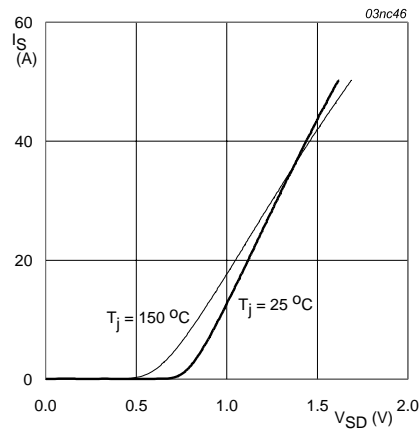
$V_{DS} = 25 \text{ V}$

**Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.**



$T_j = 25 \text{ }^\circ\text{C}; I_D = 10 \text{ A}$

**Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values.**



$V_{GS} = 0 \text{ V}$

**Fig 15. Reverse diode current as a function of reverse diode voltage; typical values.**



**9. Package outline**

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223

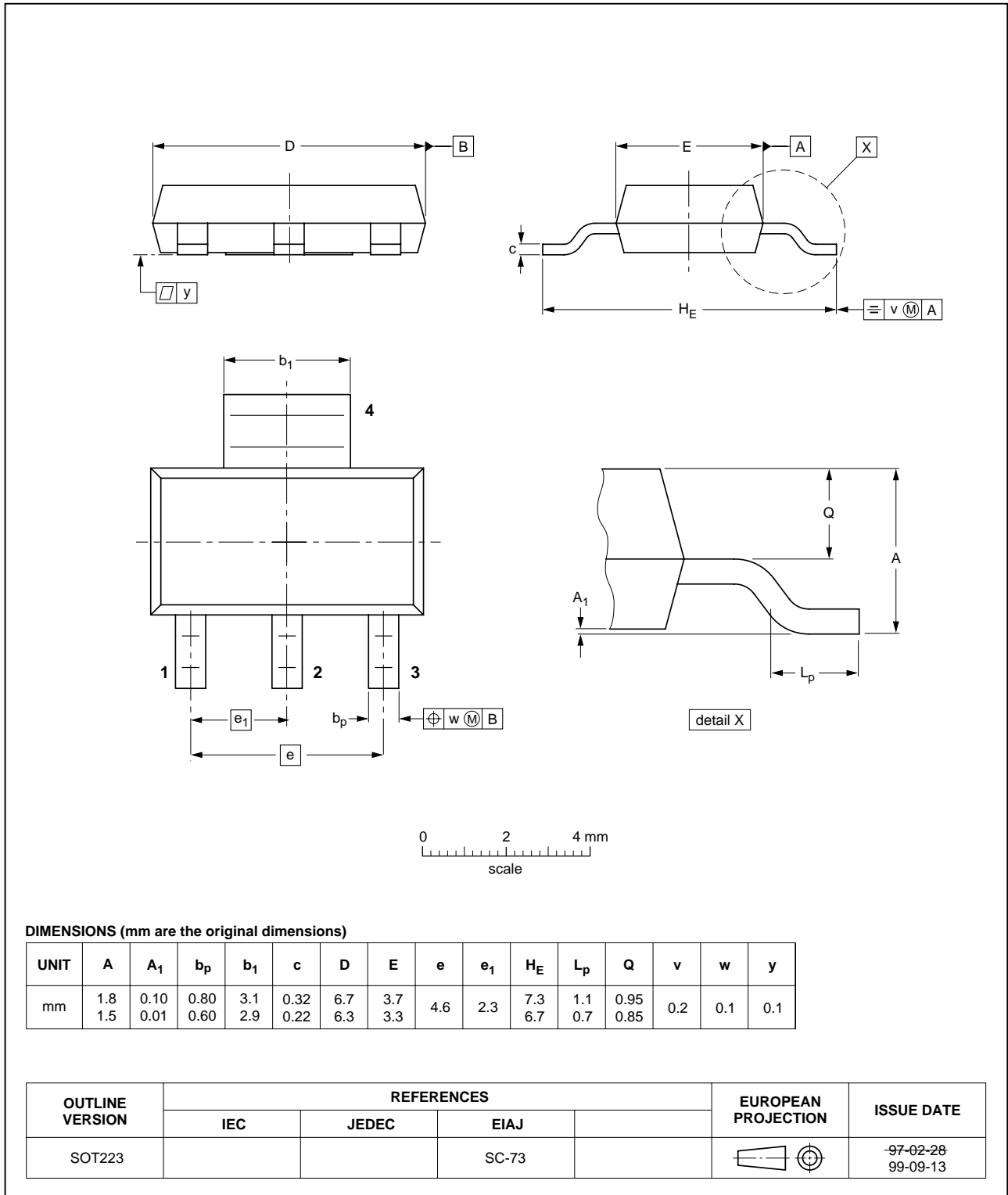
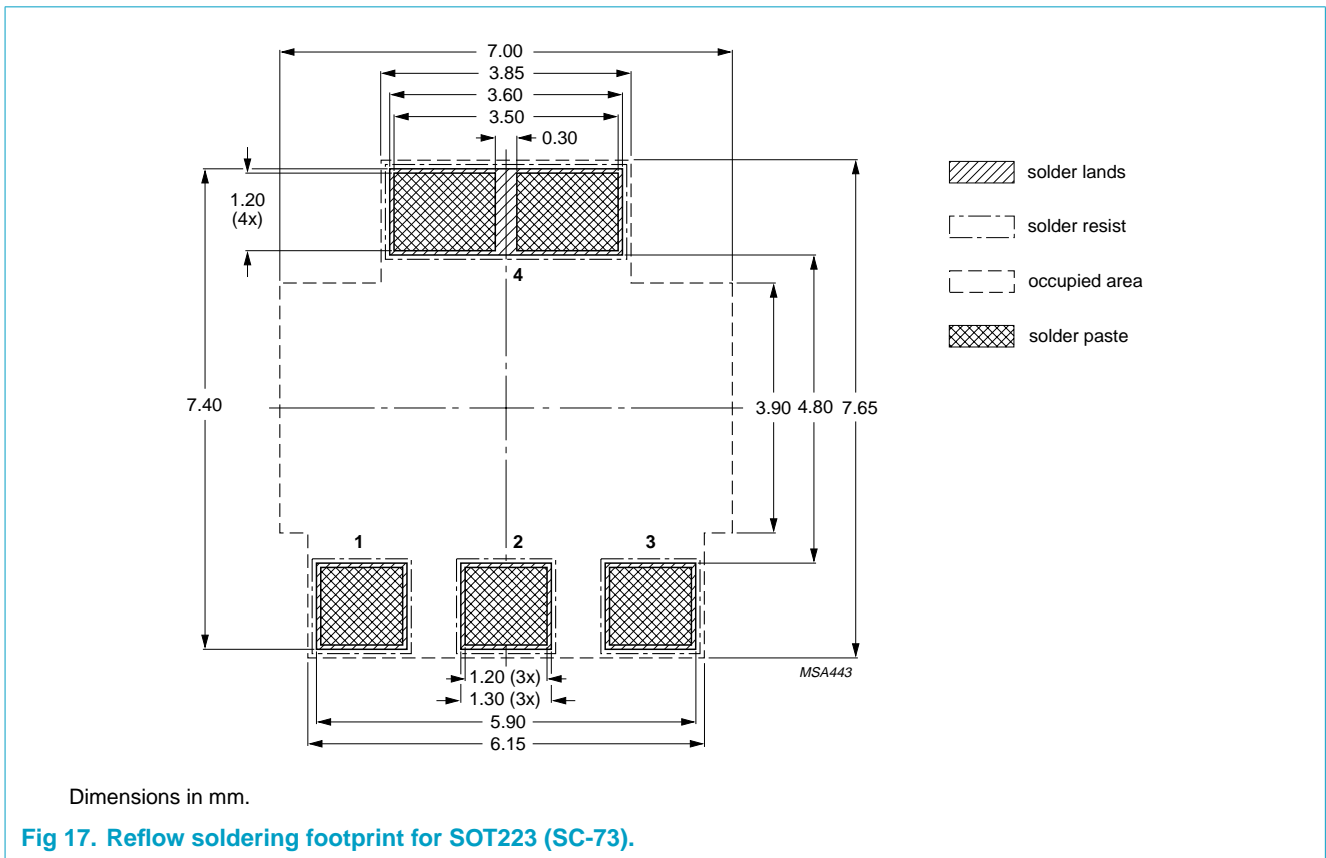


Fig 16. SOT223 (SC-73).

## 10. Soldering



## 11. Revision history

**Table 6: Revision history**

Rev	Date	CPCN	Description
01	20010207	-	Product specification; initial version.

## 12. Data sheet status

Datasheet status	Product status	Definition <sup>[1]</sup>
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

## 13. Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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**Argentina:** see South America

**Australia:** Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

**Austria:** Tel. +43 160 101, Fax. +43 160 101 1210

**Belarus:** Tel. +375 17 220 0733, Fax. +375 17 220 0773

**Belgium:** see The Netherlands

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**Bulgaria:** Tel. +359 268 9211, Fax. +359 268 9102

**Canada:** Tel. +1 800 234 7381

**China/Hong Kong:** Tel. +852 2 319 7888, Fax. +852 2 319 7700

**Colombia:** see South America

**Czech Republic:** see Austria

**Denmark:** Tel. +45 3 288 2636, Fax. +45 3 157 0044

**Finland:** Tel. +358 961 5800, Fax. +358 96 158 0920

**France:** Tel. +33 14 099 6161, Fax. +33 14 099 6427

**Germany:** Tel. +49 40 23 5360, Fax. +49 402 353 6300

**Hungary:** Tel. +36 1 382 1700, Fax. +36 1 382 1800

**India:** Tel. +91 22 493 8541, Fax. +91 22 493 8722

**Indonesia:** see Singapore

**Ireland:** Tel. +353 17 64 0000, Fax. +353 17 64 0200

**Israel:** Tel. +972 36 45 0444, Fax. +972 36 49 1007

**Italy:** Tel. +39 039 203 6838, Fax. +39 039 203 6800

**Japan:** Tel. +81 33 740 5130, Fax. +81 3 3740 5057

**Korea:** Tel. +82 27 09 1412, Fax. +82 27 09 1415

**Malaysia:** Tel. +60 37 50 5214, Fax. +60 37 57 4880

**Mexico:** Tel. +9-5 800 234 7381

**Middle East:** see Italy

**For all other countries apply to:** Philips Semiconductors,  
Marketing Communications,  
Building BE, P.O. Box 218, 5600 MD EINDHOVEN,  
The Netherlands, Fax. +31 40 272 4825

**Netherlands:** Tel. +31 40 278 2785, Fax. +31 40 278 8399

**New Zealand:** Tel. +64 98 49 4160, Fax. +64 98 49 7811

**Norway:** Tel. +47 22 74 8000, Fax. +47 22 74 8341

**Philippines:** Tel. +63 28 16 6380, Fax. +63 28 17 3474

**Poland:** Tel. +48 22 5710 000, Fax. +48 22 5710 001

**Portugal:** see Spain

**Romania:** see Italy

**Russia:** Tel. +7 095 755 6918, Fax. +7 095 755 6919

**Singapore:** Tel. +65 350 2538, Fax. +65 251 6500

**Slovakia:** see Austria

**Slovenia:** see Italy

**South Africa:** Tel. +27 11 471 5401, Fax. +27 11 471 5398

**South America:** Tel. +55 11 821 2333, Fax. +55 11 829 1849

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**Sweden:** Tel. +46 86 32 2000, Fax. +46 86 32 2745

**Switzerland:** Tel. +41 14 88 2686, Fax. +41 14 81 7730

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**Thailand:** Tel. +66 23 61 7910, Fax. +66 23 98 3447

**Turkey:** Tel. +90 216 522 1500, Fax. +90 216 522 1813

**Ukraine:** Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Tel. +44 208 730 5000, Fax. +44 208 754 8421

**United States:** Tel. +1 800 234 7381

**Uruguay:** see South America

**Vietnam:** see Singapore

**Yugoslavia:** Tel. +381 11 3341 299, Fax. +381 11 3342 553

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